IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Serial No. 10/776,101 Application of: Kim C. Hardee Filed: February 11, 2004 For: HIGH SPEED POWER-GATING TECHNIQUE FOR INTEGRATED CIRCUIT DEVICES INCORPORATING A SLEEP MODE OF OPERATION	Confirmation No.: 2835 Art Unit: 2827 Examiner: Hoang, Huan Customer No.: **25235**

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APPELLANT'S BRIEF UNDER 37 CFR § 41.37

I. Real Party in Interest

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AND

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II. Related Appeals and Interferences

No other appeals or interferences are currently known to Appellant that will directly affect, be directly affected by, or have a bearing on the decision to be rendered by the Board of Patent Appeals and Interferences in the present appeal.

III. Status of Claims

Claims 1-15 and 17-27 are pending in the application, with claim 16 being cancelled. No claims have been allowed, and all pending claims stand rejected. The rejection of claims 1-15 and 17-27 is the subject of this appeal.

IV. Status of Amendments

Appellant believes that all claim amendments have been entered.

Claims 1-15 and 17-27, including any proposed and entered claim amendments, are provided in the attached Claims Appendix.

V. Summary of Claimed Subject Matter

Independent claims 1, 5, 8, 11, 14, 17, and 19 are involved in this Appeal.

The following concise explanation of the subject matter defined in each of the independent claims 1, 5, 8, 11, 14, 17, and 19 involved in this Appeal refers to the specification by page and line numbers, and to the drawings by reference characters.

Independent claim 1 is reproduced below, annotated using reference characters and labels taken from Figures 2 and 3 of the drawings (the ground symbol is represented by the "GROUND" recitation in the annotated claims):

1. A power-gating technique for an integrated circuit device having a Sleep Mode of operation comprising:

providing an output stage (224) directly coupled between a substantially constant supply voltage source (VCC) and a substantially constant reference voltage source (GROUND); and

driving a gate terminal of at least one element of said output stage (224) to a level above (VCC + 0.3V) that of said supply voltage source

(VCC) or below (-0.3V) that of said reference voltage source (GROUND) in said Sleep Mode of operation (SLEEP).

The corresponding specification text is found in the application at page 8, line 3 through page 10, line 21.

Independent claim 5 is reproduced below, annotated using reference characters and labels taken from Figures 2 and 3 of the drawings:

5. A circuit comprising:

an output stage (224) comprising first and second series coupled transistors directly coupled between a substantially constant supply voltage source (VCC) and a substantially constant reference voltage source (GROUND), said output stage (224) comprising an input terminal (232) and an output terminal (226) thereof;

a power-gating circuit coupled to a stage preceding (220) said output stage (224) for applying a voltage level (VCC + 0.3V) to a gate terminal of said first transistor greater than that of said supply voltage source (VCC) in response to a Sleep Mode of operation (SLEEP).

The corresponding specification text is found in the application at page 8, line 3 through page 10, line 21.

Independent claim 8 is reproduced below, annotated using reference characters and labels taken from Figures 2 and 3 of the drawings:

8. A circuit comprising:

an output stage (224) comprising first and second series coupled transistors directly coupled between a substantially constant supply voltage source (VCC) and a substantially constant reference voltage

source (GROUND), said output stage (224) comprising an input terminal (232) and an output terminal (226) thereof;

a power-gating circuit (244) coupled to a stage preceding (220) said output stage (224) for applying a voltage level (-0.3V) to a gate terminal of said second transistor lesser than that of said reference voltage source (GROUND) in response to a Sleep Mode of operation (SLEEP).

The corresponding specification text is found in the application at page 8, lines 3 through 32.

Independent claim 11 is reproduced below, annotated using reference characters and labels taken from Figures 2 and 3 of the drawings:

11. An integrated circuit device including a power-gated write data driver circuit for a memory array, said driver circuit comprising:

at least a first stage (218) coupled between a substantially constant supply voltage source (VCC) and a power-gated reference voltage line (206);

an output stage (224) directly coupled between said supply voltage source (VCC) and a substantially constant reference voltage source (GROUND), an input 232 to said output stage (224) being coupled to an output of said at least said first stage (220); and

a power-gating circuit (244) coupled to a stage preceding (220) said output stage (224) for driving said input to a level lower (-0.3V) than that of said reference voltage source level (GROUND) in response to a Sleep Mode of operation (SLEEP).

The corresponding specification text is found in the application at page 8, lines 3 through 32.

Independent claim 14 is reproduced below, annotated using reference characters and labels taken from Figures 2 and 3 of the drawings:

> 14. An integrated circuit device including a power-gated write data driver circuit for a memory array, said driver circuit comprising:
>
> at least a first stage (220) coupled between a substantially constant reference voltage source (GROUND) and a power-gated supply voltage line (204);
>
> an output stage (224) directly coupled between a substantially constant supply voltage source (VCC) and said reference voltage source (GROUND), an input to said output stage being coupled to an output of said at least said first stage; and
>
> a power-gating circuit coupled to said input of said output stage for driving said input to a level higher (VCC + 0.3V) than that of said supply voltage source level (VCC) in response to a Sleep Mode of operation (SLEEP).

The corresponding specification text is found in the application at page 8, lines 3 through 32.

Independent claim 17 is reproduced below, annotated using reference characters and labels taken from Figures 2 and 3 of the drawings:

> 17. A power-gating technique for an integrated circuit device having a Sleep Mode of operation comprising:
>
> providing an output stage (224) directly coupled between a substantially constant supply voltage source (VCC) and a substantially constant reference voltage source (GROUND); and

driving a common gate terminal of said output stage to a level above that (VCC + 0.3V) of said supply voltage source (VCC) in said Sleep Mode of operation (SLEEP).

The corresponding specification text is found in the application at page 8, lines 3 through 32.

Independent claim 19 is reproduced below, annotated using reference characters and labels taken from Figures 2 and 3 of the drawings:

19. A power-gating technique for an integrated circuit device having a Sleep Mode of operation comprising:

providing an output stage (224) directly coupled between a substantially constant supply voltage source (VCC) and a substantially constant reference voltage source (GROUND); and

driving a common gate terminal of said output stage to a level below that (-0.3V) of said reference voltage source (GROUND) in said Sleep Mode of operation (SLEEP).

The corresponding specification text is found in the application at page 8, lines 3 through 32.

VI. Grounds of Rejection to be Reviewed on Appeal

Claims 1-15 and 17-27 stand rejected under 35 USC 102(e) as being anticipated by Hidaka et al (US Patent No. 6,635,934).

VII. Argument

The rejection of claims 1-15 and 17-27 under 35 USC 102(e) as being anticipated by Hidaka is improper.

The rejection of claims 1-15 and 17-27 under 35 USC 102(e) is respectfully traversed and the arguments presented in the Amendment after Final Office Action filed on June 4, 2007 are maintained.

It is well settled that a patent claim is invalid as anticipated under 35 USC 102(e) if every limitation in a claim is found in a single prior art reference, either explicitly or inherently. All claim limitations must be considered, and none can be selectively ignored.

Applicant continues to assert that there are clear differences between the present invention as claimed, and the invention taught by Hidaka. Applicant stands by the arguments made in the previous response regarding the pertinent node voltages taught by Hidaka:

> Hidaka teaches an internal circuit node voltage Vccs, which is clearly shown in FIG. 19. The actual power supply is Vcc, which is a normal external power supply having a substantially constant voltage level, and is not generated by the circuit itself. In contrast, the internal voltage, Vccs, is generated by a P-channel transistor, which is in turn switched by the gate voltage signal designated "Φ". In effect, the internal voltage Vccs is merely an internal signal node or a power-gated supply line with a varying voltage signal. Evidence of this is given in the immediately adjacent timing diagram of FIG. 20, in which Vccs is shown to be a switched signal and not a "supply voltage source" as claimed. (emphasis added)

In an attempt to obtain the allowance of claims 1-15 and 17-27, each of the independent claims 1, 5, 8, 11, 14, 17, and 19 were restricted so that the supply voltage source cannot be more broadly interpreted than was originally intended. Each of the independent claims has been amended to recite that the supply voltage source provides a "substantially constant" power supply voltage and not a switched internal circuit signal or

gated power supply voltage as taught in Hidaka. Similarly, independent claims 1, 5, 8, 11, 14, 17, and 19 were amended to claim a "substantially constant" reference voltage source to prevent the reference voltage source from being more broadly interpreted than was originally intended.

The Examiner's comments regarding these arguments are respectfully traversed.

Firstly, the fact that the claims do not recite "any external power supply" is not relevant to the patentability of the claims. Applicant is not relying on the naked internal/external power supply distinction, which perhaps would have been separately challenged, but rather on the objective, demonstrable distinction between a circuit node voltage that is "substantially constant" versus a circuit node voltage that is not substantially constant. The term "substantially constant" is used to make explicit what most persons of ordinary skill in the art already view as a feature of a supply voltage or a reference voltage and is being used specifically to overcome the teachings of the Hidaka reference. Typically, external power supply voltages are "substantially constant." Sometimes internally generated power supply voltages are not substantially constant but are switched in and out as is the case in Hidaka. The full sentence in question referred to by the Examiner is:

> The actual power supply is Vcc, which is a normal external power supply having a substantially constant voltage level, and is not generated by the circuit itself. (emphasis added)

Thus, it can be seen that the claims were amended to include a bona fide claim limitation associated with external power supply voltages and reference voltages and there is no need to include the term "external."

Secondly, the Examiner's own argument "substantially constant (Standby period only)" is self-refuting. The term "substantially constant" would be clear to those skilled in the art, especially with respect to power supply voltages and reference voltages, i.e. providing a constant voltage with minor variations due to noise and glitches.

Intentionally switching an internal supply voltage in and out between different voltage levels during different operating modes cannot be said to be consistent with the term "substantially constant."

This is not to say that a "substantially constant reference voltage" cannot be switched in and out of a circuit. However, the correct usage in a claim would then be to recite explicitly when the "substantially constant reference voltage" appears and when it does not. When it does appear, it does not switch, but is "constant". For example, a proper claim construction might be a "substantially constant reference voltage applied to an output when the input is high" or a "substantially constant reference voltage available when the input is low" or the like. The use of the term "substantially constant reference voltage" without more would be known by those skilled in the art to mean that it is available at all times and is not switched in and out. The claim should be interpreted as including an unchanging reference voltage unless specific claim language is provided to specify when the reference voltage is available and when it is not.

Thirdly, the term "substantially constant reference voltage" is routinely used in patents to describe an unchanging reference voltage of the type being asserted by the Appellant, or specifies the operational mode time constraints within the claim itself. Appellant could not find an instance where "substantially constant reference voltage" by itself, as used in the present appeal, referred to a switched reference voltage. The following list is not exhaustive, but undoubtedly many more such examples bolstering the Appellant's position could easily be found.

US Patent 7,148,742 to Pan et al uses the term "substantially constant reference voltage" in claims 35 and 37 to claim a bandgap voltage that is unchanging during the time which it is present at the output. There are no modes of operation while the voltage is characterized as a "substantially constant reference voltage". Claim 35 characterizes the reference voltage in time with the specific claim language.

US Patent 7,151,679 to Strijker uses the term "substantially constant reference voltage" consistent with the meaning asserted by the Appellant in claim 15.

US Patent 7,164,308 to Lee shows a "substantially constant reference voltage" as an unchanging Vref voltage in Figure 3 thereof.

US Patent 7,170,394 to Chandler et al defines "substantially constant" for characterizing a "substantially constant reference voltage" as a "voltage potential across the wire pair that is supplied to the remote device remains essentially fixed subject to a small margin of error." This is precisely in keeping with the Appellant's suggested definition of an unchanging reference voltage subject to noise, glitches, and small margins of error unless specific claim language is set forth to characterize the presence and absence of the reference voltage by being acted upon by external switching circuitry or the like.

US Patent 7,176,739 to Devine et al uses the term "substantially constant reference voltage" in claim 1 to describe the unchanging reference voltage at node 307 in Figures 3 and 4 that is consistent with the term definition suggested by the Appellant.

US Patent 7,209,060 to Kumar et al uses the term "substantially constant reference voltage" in claim 13 to describe a switched reference voltage, but claim 13 includes the further limiting term "in a plurality of time durations".

Fourthly, there is no prohibition under §112, second paragraph from using qualitative or relative terms, such as "about," "substantially," "essentially," to qualify claimed elements. The test is whether one of average skill in the art, either from reading the written description, prosecution history or from a knowledge of the art in general, would understand the meaning of the term and could ascribe general upper and lower limits. *Amgen, Inc. v. Chugai Pharmaceutical Co., Ltd.*, 927 F.2d 1200, 1217-18 (Fed. Cir. 1991); *Andrew Corp. v. Gabriel Electronics*, 847 F.2d 819, 821 (Fed. Cir. 1988.

It is deemed that one of ordinary skill in the art would know that "substantially constant reference voltage" in the context of the present invention means "constant but subject to minor variation due to noise and glitches and the like", as an absolute constant voltage is impossible in an actual implementation.

Claims 1, 5, 8, 11, 14, 17, and 19, therefore, are still deemed to be allowable as containing a limitation not taught in the Hidaka reference. The remaining claims are

deemed to be allowable as being dependent from an allowable base claim for the reasons given above.

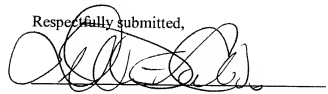
For the reasons given above, the rejection of claims 1-2, 4-6, 8-9 and 20 under 35 USC § 102(e) as being anticipated by Chliwnyj et al is improper and should be reversed.

Conclusion

In view of all of the above, claims 1-15 and 17-27 are believed to be allowable and the case in condition for allowance. Appellant respectfully requests that the Examiner's rejections based on 35 U.S.C. § 102(e) be reversed for the pending claims.

Date: 31 August 2007

Respectfully submitted,



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VIII. CLAIMS APPENDIX

1. A power-gating technique for an integrated circuit device having a Sleep Mode of operation comprising:

providing an output stage directly coupled between a substantially constant supply voltage source and a substantially constant reference voltage source; and

driving a gate terminal of at least one element of said output stage to a level above that of said supply voltage source or below that of said reference voltage source in said Sleep Mode of operation.

2. The power-gating technique of claim 1 wherein said output stage comprises series coupled P-channel and N-channel transistors coupled between said supply voltage source and said reference voltage source.

3. The technique of claim 2 wherein said gate terminal of said N-channel transistor is driven below said reference voltage level while in said Sleep Mode of operation.

4. The technique of claim 2 wherein said gate terminal of said P-channel transistor is driven above said supply voltage level while in said Sleep Mode of operation.

5. A circuit comprising:

an output stage comprising first and second series coupled transistors directly coupled between a substantially constant supply voltage source and a substantially constant reference voltage source, said output stage comprising an input terminal and an output terminal thereof;

a power-gating circuit coupled to a stage preceding said output stage for applying a voltage level to a gate terminal of said first transistor greater than that of said supply voltage source in response to a Sleep Mode of operation.

6. The circuit of claim 5 wherein said output stage comprises a CMOS inverter and said first transistor comprises a P-channel transistor.

7. The circuit of claim 5 wherein said voltage level applied to said gate terminal of said first transistor comprises substantially said supply voltage source level plus 0.3V.

8. A circuit comprising:

an output stage comprising first and second series coupled transistors directly coupled between a substantially constant supply voltage source and a substantially constant reference voltage source, said output stage comprising an input terminal and an output terminal thereof;

a power-gating circuit coupled to a stage preceding said output stage for applying a voltage level to a gate terminal of said second transistor lesser than that of said reference voltage source in response to a Sleep Mode of operation.

9. The circuit of claim 8 wherein said output stage comprises a CMOS inverter and said second transistor comprises a N-channel transistor.

10. The circuit of claim 8 wherein said voltage level applied to said gate terminal of said second transistor comprises substantially said reference voltage source level minus 0.3V.

11. An integrated circuit device including a power-gated write data driver circuit for a memory array, said driver circuit comprising:

at least a first stage coupled between a substantially constant supply voltage source and a power-gated reference voltage line;

an output stage directly coupled between said supply voltage source and a substantially constant reference voltage source, an input to said output stage being coupled to an output of said at least said first stage; and

a power-gating circuit coupled to a stage preceding said output stage for driving said input to a level lower than that of said reference voltage source level in response to a Sleep Mode of operation.

12. The integrated circuit device of claim 11 wherein said output stage comprises a CMOS inverter comprising at least one series coupled P-channel transistor and at least one N-channel transistor.

13. The integrated circuit device of claim 12 wherein a gate terminal of said at least one N-channel transistor is driven to establish a negative V_{GS} in response to said Sleep Mode of operation.

14. An integrated circuit device including a power-gated write data driver circuit for a memory array, said driver circuit comprising:

at least a first stage coupled between a substantially constant reference voltage source and a power-gated supply voltage line;

an output stage directly coupled between a substantially constant supply voltage source and said reference voltage source, an input to said output stage being coupled to an output of said at least said first stage; and

a power-gating circuit coupled to said input of said output stage for driving said input to a level higher than that of said supply voltage source level in response to a Sleep Mode of operation.

15. The integrated circuit device of claim 14 wherein said output stage comprises a CMOS inverter comprising at least one series coupled P-channel transistor and at least one N-channel transistor.

17. A power-gating technique for an integrated circuit device having a Sleep Mode of operation comprising:

providing an output stage directly coupled between a substantially constant supply voltage source and a substantially constant reference voltage source; and

driving a common gate terminal of said output stage to a level above that of said supply voltage source in said Sleep Mode of operation.

18. The power-gating technique of claim 17 wherein said output stage comprises series coupled P-channel and N-channel transistors coupled between said supply voltage source and said reference voltage source, and to the common gate terminal.

19. A power-gating technique for an integrated circuit device having a Sleep Mode of operation comprising:

providing an output stage directly coupled between a substantially constant supply voltage source and a substantially constant reference voltage source; and

driving a common gate terminal of said output stage to a level below that of said reference voltage source in said Sleep Mode of operation.

20. The power-gating technique of claim 19 wherein said output stage comprises series coupled P-channel and N-channel transistors coupled between said supply voltage source and said reference voltage source, and to the common gate terminal.

21. The technique of claim 1 wherein the output stage comprises two transistors directly coupled to an output terminal of the output stage.

22. The circuit of claim 5 wherein the output stage comprises two transistors directly coupled to the output terminal of the output stage.

23. The circuit of claim 8 wherein the two transistors in the output stage are directly coupled to the output terminal of the output stage.

24. The circuit of claim 11 wherein the output stage comprises two transistors directly coupled to an output terminal of the output stage.

25. The circuit of claim 14 wherein the output stage comprises two transistors directly coupled to an output terminal of the output stage.

26. The technique of claim 17 wherein the output stage comprises two transistors directly coupled to an output terminal of the output stage.

27. The technique of claim 19 wherein the output stage comprises two transistors directly coupled to an output terminal of the output stage.

IX. EVIDENCE APPENDIX

No copies of evidence are required with this Appeal Brief. Appellant has not relied upon any evidence submitted under 37 C.F.R. §§ 1.130, 1.131, or 1.132.

X. RELATED PROCEEDINGS APPENDIX

There are no copies of decisions rendered by a court or the Board to provide with this Appeal as there are no related proceeding.